Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**91 mils**

**70 mils**

**GATE**

**SOURCE**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: S = .018” X .025” G = .019” X .025”**

**Backside Potential: Drain**

**Geometry: GEN 3**

**Mask Ref: HEX 1, 100V, P-Channel**

**APPROVED BY: DK DIE SIZE .070” X .091” DATE: 9/22/21**

**MFG: IR THICKNESS .010” P/N: IRFC9110**

**DG 10.1.2**

#### Rev B, 7/19/02